Due to the continuous progress in nano-scale technology highly complex systems can nowadays be integrated into a single chip or package, and emerging approaches for the 3D-integration of densely coupled chip-stacks provide the basis for manifold new applications. Meanwhile, systems-in-a-package (SiP) and networks-on-a-chip (NoC) constitute the core components of many applications ranging from consumer electronics to extremely safety critical systems, e.g. in automotive or medical electronics.

However, at the same time, shrinking feature sizes come along with severe problems in design, verification, and test of integrated circuits and systems. On the one hand, manufacturing processes are getting more vulnerable against small disturbances, and on the other hand, manufactured chips are getting more susceptible to external noise ("soft errors") and dynamic parameter variations. For example, the limited resolution of sub wavelength lithography may lead to variations in the chip geometry, which in turn may cause variations of the circuit parameters including the threshold voltage of transistors. During system operation “hot spots” due to increased switching activities in certain areas of a chip may for example cause voltage droops. Both process-related and dynamic variations manifest themselves as variations of the circuit timing, such that timing analysis and verification has gained increasing importance. Moreover, long term parameter variations, such as ageing effects, make it difficult to find the optimum design solution with respect to area, performance, and reliability.

Traditional design approaches based on worst-case or average-case decisions do not consider parameter variations and cannot fully exploit the potential of nano-scale technologies because of unnecessarily high safety margins. Thus, design has undergone a paradigm shift towards “statistical” and “variation-aware” design. Statistical design relies on probability density functions of the relevant circuit parameters when analyzing and optimizing the design. Robust and variation-aware architectures try to compensate both parameter variations and soft errors to a certain extent.

Approaching design from this new angle is associated with a variety of challenges. First of all realistic probability density functions must be determined which characterize the circuit behavior as precisely as possible. Robust and variation-aware systems have to efficiently combine error and variation tolerance at all levels of the design, and they must be appropriately tuned to the specific requirements of the targeted application. Furthermore, design validation and verification must particularly address the robustness and fault tolerance properties of a system. Throughout the life cycle of a system, efficient offline and online tests are necessary to screen out defective devices and to detect errors before they can corrupt the system function. On top of that, testing a robust system is especially difficult, as critical defects must be distinguished from tolerable variations and disturbances. The contributions of this special issue highlight these challenges and present some exemplary solutions.

The first article by Lorenz, Georgakos, and Schlichtmann presents a pioneering approach to analyze and model the impact of NBTI (Negative Bias Temperature Instability) and HCI (Hot Carrier Injection) on the circuit behavior over time. It is based on a probabilistic model, which characterizes the stress conditions responsible for NBTI and HCI. Combined with information about the circuit temperature, the supply voltage, and the transistor dimensions, this model provides the expected delay degradations and signal shapes induced by NBTI and HCI. The resulting ageing model at gate level thus supports considerably more precise estimations than previously used worst-case predictions.

Subsequently, Polian and Becker discuss fault models for manufacturing defects in nano-scale CMOS and present dedicated algorithms for fault simulation and automatic test pattern generation (ATPG). The described models range from interconnect-open defects over resistive bridges and power-droop defects to the conditional multiple stuck-at fault model (CMS@), which provides

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a flexible framework for uniquely representing a variety of different fault models. Fault simulation of resistive bridges requires for example an efficient manipulation of so-called analogue detectability intervals describing the resistance ranges where bridges are detected by certain patterns. ATPG for the presented advanced models must for example be able to handle constraints effectively.

Next, Gebelein, Engel, and Kebschull focus on Field Programmable Gate Arrays (FPGAs) used in measurement units for high-energy-physics experiments. To mitigate radiation-induced soft errors in such a harsh environment at reasonable cost, a multi-level approach is followed. This comprises for example the periodic refreshment ("scrubbing") of the configuration SRAMs and a specially designed RISC processor as the basis of the operating system. At the application level SoftWare Implemented Fault Tolerance (SWIFT) provides a low-cost solution.

The following two contributions deal with fault tolerance at the network and at the algorithmic level. Schley, Radetzki, and Kohler present a routing algorithm supporting the graceful degradation of network switches. To reduce the impact of failures in network switches, they propose to turn-off only the affected ports. For an optimal rerouting of the network traffic a fault-adaptive cost-based routing algorithm is introduced. The scheme for algorithmic fault tolerance suggested by Braun and Wunderlich adapts earlier concepts of exploiting inherent check information in algorithms for matrix multiplication to parallelized implementations on many-core architectures. The proposed distributed checking scheme ensures a high fault tolerance while keeping the impact on computing performance low.

Finally, Fey, Süßlow, Frehse, and Drechsler address the problem of robustness verification. They present a formal approach to determine the fault tolerance of combinatorial and sequential circuits with respect to soft errors. The underlying circuit model uses a limited time frame extension, and by attaching error predicates to circuit components, the circuit can be efficiently partitioned into robust and non-robust components. A failure of a robust component doesn’t change the system function and can be tolerated, while the list of non-robust components can be used as a guideline for further circuit hardening or additional fault tolerance measures.

At last, I would like to thank all the authors for submitting their manuscripts to this special issue and the reviewers for their invaluable contributions to the reviewing process. I would also like to thank the Editor-in-Chief, Professor Paul Molitor, for giving me the great opportunity of organizing this special issue.

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